Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to further make explicit the claims as originally claimed and disclosed.

Support for the amendments is found in the original claims, the Figures (1 and 2) and the Specification, e.g., paragraphs 0025 and 0028:

"Fig. 2 shows a pattern of travel for the electrical probe tip 16 with respect to the microelectronic product 14 when electrically stressing the microelectronic product 14 at other than an electrical contact portion of the microelectronic product 14. In accord with Fig. 2, the electrical probe tip 16 stress pattern is serpentine. **The electrical probe tip 16 may be picked and placed when simultaneously electrically stressing and electrically testing the microelectronic product** 14. Alternatively, the electrical probe tip 16 may be dragged along the surface of the microelectronic product 14, provided that the microelectronic product 14 is not coincidentally damaged thereby."

"Fig. 4A shows the microelectronic product 14 generally in accord with Fig. 2 and the electrical probe tip 16 positioned thereupon, electrically biased and intended to be traced in a serpentine fashion over the

microelectronic product 14 which has formed therein a circuit element 25. **By simultaneously scanning the electrical probe tip 16 over the microelectronic product 14 while electrically testing the microelectronic product** in accord with a differentiation of the timing diagrams of Fig. 3A and Fig. 3B, defective portions of the circuit element 25 may be mapped. Such mapped portions are illustrated in Fig. 4B as defective circuit element portions 25'."

Claim Rejections under 35 USC 102

1. Claims 1-6, 8-13, 15-18 and 20 stand rejected under 35 USC Section 102(b) as being anticipated by Ishii et al. (US 5,493,236).

Ishii et al. disclose a test analysis apparatus for optical beam induced current (OBIC) and luminous analysis from a rear surface of a semiconductor wafer (see Abstract). In the method and apparatus of Ishii a test pulse signal is supplied to respective **electrode pads (electrical contact portions)** on the front surface of the wafer (see Abstract; col 6, lines 43-47; lines 56-64) to actuate the semiconductor wafer circuitry while at the same time attempting to detect a current generated in the circuitry from a defective portion of the circuitry (e.g., P-N junctions col 2, lines 55). **Simultaneously the semiconductor wafer is irradiated from the rear side** and any luminosity from

the semiconductor wafer is detected (see col 3, lines 43-60; col 4, lines 19-28).

Thus Ishii et al. fails to disclose several aspects of Applicants disclosed and claimed invention including:

"a **movable electrical probe tip separated from said electrical test head and positionable with respect to the electrical test head such as to electrically stress a portion of the microelectronic product other than an electrical contact portion of the microelectronic product** while said electrical test head is **simultaneously positionable to electrically contact said electrical contact portion** to produce electrical test data for said microelectronic product."

Ishii et al. fail to disclose anywhere an electrical probe tip as Applicants have disclosed and claimed.

As noted, Ishii et al. disclose a probe tip that is **part of a single test head** that is positionable applying an electrical Voltage to an **electrical contact portion (electrode pads)** to actuate a semiconductor device.

Examiner does not refer to any part of the disclosure of Ishii et al. to support his assertion that Ishii et al. disclose the elements of Applicants invention other than referring to item (20) which generally defines the semiconductor wafer under test (see Fig 2).

"Examiner is required to interpret the claims by giving the terms thereof the broadest reasonable interpretation in their ordinary usage as they would be understood by one of ordinary skill in the art in light of the written specification, including drawings, unless another meaning is intended by appellants as established in the written specification, and without reading into the claims any limitation or particular embodiment disclosed in the specification." *See e.g., In re Morris*, 127 F.3d. 1048, 1054-55, 44 USPQ2d 1023, 1027 (Fed. Cir 1997); *In re Zeltz* (893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Ishii et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention as claimed in both Applicants independent claims and dependent claims.

"A claim is anticipated only if each and every element as

set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Further, with respect to claims 9 and 16, nowhere do Ishii et al. disclose:

"sequentially **movably positioning the electrical probe tip to sequential positions comprising said other than an electrical contact portion** of the semiconductor product and electrically stressing the microelectronic product with said electrical probe tip **while simultaneously electrically testing the microelectronic product with said electrical test head contacting said electrical contact portion** to produce said electrical test data for said microelectronic product."

Claim Rejections under 35 USC 103

2. Claims 7, 14, and 19 stand rejected under 35 USC Section 103(a) as being unpatentable over by Ishii et al., above, in view of Ohno et al. (US 5,091,662).

Applicants reiterate the comments made above with respect to Ishii et al.

Ohno et al., like, Ishii et al., also teach **applying a test signal to electrode pads (electrical contact portions)** with a plurality **of test probes** (see Abstract) where the object of the invention is to provide a wafer probing test machine capable of **positioning the electrical probes on the pads (electric contact portions) with higher accuracy** (see Abstract; col7, lines 40-59).

Thus, even assuming arguendo, a proper motivation for combining the teachings of Ishii et al. and Ohno et al., such combination does not produce Applicants disclosed and claimed

invention.

"Finally, the prior art reference (or references when combined) must teach or suggest **all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

Since the cited references, singly or in combination, fail to produce Applicants disclosed and claimed invention, such references fail to make out a *prima facie* case of anticipation or obviousness with respect to both Applicants independent claims and dependent claims.

Based on the foregoing, Applicants respectfully request that Examiner reconsider Applicants claims to find that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in

a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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